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IN THE CLAIMS:

Claim 1 (Currently Amended) A bulk silicon etching method comprising the following steps in the order named ~~of~~:

(a) providing a silicon wafer;

(b) diffusing the wafer with dopant, whereby the diffusion creates a PN-junction at a predetermined PN-junction depth throughout the surface of the wafer;

(c) providing a mask;

(d) positioning the mask in overlying relation to the surface of the wafer;

(e) patterning a layer of oxide on the surface of the wafer, whereby the pattern of the oxide layer is defined by the mask;

(f) etching the wafer to create ~~recessed areas~~ recesses in the wafer in the areas that are not patterned with the oxide layer ~~coincident with the patterned oxide~~, whereby the etching step is sufficient to etch away the ~~surface~~ wafer to a depth below the PN-junction depth created by the diffusion step, thereby creating recessed areas having sidewalls, the sidewalls characterized by the presence of the PN-junction above the PN-junction depth and the absence of ~~surface~~ the PN-junction below the PN-junction depth;

(g) hydrofluoric acid etching the wafer to form porous silicon thereon, whereby the porous silicon is formed ~~coincident with~~ in the ~~surface wafer~~ sidewalls of the recessed areas characterized by the absence of ~~surface~~ the PN-junction; and

(h) subjecting the wafer ~~surface~~ to wet etching resulting in dissolution of the porous silicon.

Claim 2 (Previously Cancelled)

Claim 3 (Previously Cancelled)

Claim 4 (Original) The method of claim 1, wherein the silicon wafer is an N-type silicon wafer.